Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) An electronic device, comprising:

an electronic component; and

an integrated circuit configured to generate a system clock, an external clock having a programmable delay from the system clock and a feedback clock having a programmable delay, the integrated circuit being further configured to provide the external clock to the electronic component to support communications therewith, communicate with the electronic component, and calibrate the external clock delay as a function of the communications, wherein the communications comprise a plurality of transmissions between the integrated circuit and the electronic component, the integrated circuit being further configured to program a different external clock delay for each of the transmissions, to communicate each of the transmissions between the integrated circuit and the electronic component in response to the corresponding different external clock delays, to record timing parameters associated with each of the transmissions communicated between the integrated circuit and the electronic component in response to the communication of each of the transmissions, the integrated circuit is further configured to program the external clock delay and the feedback clock delay with a fixed offset between the external and feedback clocks for each of read/write operations, and calibrate the external clock delay and the feedback clock delay with the fixed offset between the external and feedback clocks, the integrated circuit being further configured to calibrate the external clock delay and the feedback clock delay by determining the lowest delay between the system clock and one of the external and feedback clocks for a successful read/write operation and the highest delay between the system clock and said one of the external and feedback clocks for the successful read/write operation, and selecting a delay comprising the center value between the lowest delay and the highest delay, the selected delay being used to calibrate said one of the external and feedback clocks, and to calibrate the external clock delay as a function of the recorded timing parameters for each of the transmissions to support future communications between the integrated circuit and the electronic component.

2. (Cancelled)

3. (Original) The electronic device of claim 1 wherein the electronic component comprises memory.

4. (Original) The electronic device of claim 3 wherein the integrated circuit is further configured to use the external clock to write to and read from the memory, and use the feedback clock to sample data read from the memory.

5. (Original) The electronic device of claim 4 wherein the integrated circuit is further configured to calibrate the feedback clock delay as a function of the communications.

6. (Original) The electronic device of claim 5 wherein the communications comprise a plurality of read/write operations, the integrated circuit being further configured to program a different external clock delay and a different feedback clock delay for each of the read/write operations, and calibrate the external clock delay and the feedback clock delay as a function of the read/write operations.

7-9. (Cancelled)

10. (Original) The electronic device of claim 3 wherein the memory comprises a Synchronous Dynamic Random Access Memory (SDRAM).

11. (Original) The electronic device of claim 1 wherein the electronic device comprises a wireless telephone.

12. (Previously Presented) A method of calibrating an integrated circuit to an electronic component, the integrated circuit having a system clock, comprising:

generating an external clock on the integrated circuit, the external clock having a programmable delay from the system clock;

providing the external clock from the integrated circuit to the electronic component to support communications therewith;

programming a different external clock delay for each of a plurality of transmissions;

communicating each of the plurality of transmissions between the integrated circuit and the electronic component in response to the corresponding different external clock delays;

recording timing parameters associated with each of the transmissions communicated between the integrated circuit and the electronic component in response to the communication of each of the transmissions,

calibrating the external clock delay as a function of the recorded timing parameters for each of the transmissions to support future communications between the integrated circuit and the electronic component; and

generating a feedback clock on the integrated circuit, the feedback clock having a programmable delay from the system clock, and wherein the communications between the integrated circuit and the electronic component further comprise using the external clock to write to and read from the electronic component, and using the feedback clock to sample, at the integrated circuit, data read from the electronic component, wherein the external clock delay and the feedback clock delay are programmed with a fixed offset there between for each of read/write operations, and wherein the external clock delay and the feedback clock delay are calibrated with the fixed offset there between, wherein the calibration of the external clock delay and the feedback clock delay further comprises determining the lowest delay between the system clock and one of the external and feedback clocks for the successful read/write operation and the highest delay between the system clock and said one of the external and feedback clock for a successful read/write operation, and selecting a delay comprising the center value between the lowest delay and the highest delay, the selected delay being used to calibrate said one of the external and feedback clocks.

13. (Cancelled)

14. (Original) The method of claim 12 wherein the electronic component comprises memory.

15. (Cancelled)

16. (Original) The method of claim 14 further comprising calibrating the feedback clock delay as a function of the communications.

17. (Original) The method of claim 16 wherein the communications between the integrated circuit and the memory comprise a plurality of read/write operations, the method further comprising programming a different external clock delay and a different feedback

clock delay for each of the read/write operations, and wherein the calibration of the external clock delay and the feedback clock delay is a function of the read/write operations.

18-20. (Cancelled)

21. (Original) The method of claim 14 wherein the memory comprises a Synchronous Dynamic Random Access Memory (SDRAM).

22. (Original) The method of claim 12 wherein the integrated circuit and the electronic component form at least part of a wireless telephone.

23-24. (Cancelled)

25. (Previously Presented) Computer readable media embodying a program of instructions executable by a processor to perform a method of calibrating an integrated circuit to an electronic component, the integrated circuit including a system clock and an external clock having a programmable delay from the system clock, the external clock being provided to the electronic component to support communications therewith, the method comprising:

programming a different external clock delay for each of a plurality of transmissions;

communicating each of the plurality of transmissions between the integrated circuit and the electronic component in response to the corresponding different external clock delays;

recording timing parameters associated with each of the transmissions communicated between the integrated circuit and the electronic component in response to the communication of each of the transmissions; and

calibrating the external clock delay as a function of the recorded timing parameters for each of the transmissions to support future communications between the integrated circuit and the electronic component, generating a feedback clock on the integrated circuit, the feedback clock having a programmable delay from the system clock, and wherein the communications between the integrated circuit and the electronic component further comprise using the external clock to write to and read from the electronic component, and using the feedback clock to sample, at the integrated circuit, data read from the electronic component, wherein the external clock delay and the feedback clock delay are programmed with a fixed offset therebetween for each of read/write operations, and wherein the external

clock delay and the feedback clock delay are calibrated with the fixed offset therebetween, wherein the calibration of the external clock delay and the feedback clock delay further comprises determining the lowest delay between the system clock and one of the external and feedback clocks for a successful read/write operation and the highest delay between the system clock and said one of the external and feedback clocks for the successful read/write operation, and selecting a delay comprising the center value between the lowest delay and the highest delay, the selected delay being used to calibrate said one of the external and feedback clocks.

26. (Original) The computer readable media of claim 25 wherein the electronic component comprises memory, and the method further comprises calibrating the feedback clock delay as a function of the communications.

27. (New) An integrated circuit having a system clock, comprising:

means for generating an external clock on the integrated circuit, the external clock having a programmable delay from the system clock;

means for providing the external clock from the integrated circuit to the electronic component to support communications therewith;

means for programming a different external clock delay for each of a plurality of transmissions;

means for communicating each of the plurality of transmissions between the integrated circuit and the electronic component in response to the corresponding different external clock delays;

means for recording timing parameters associated with each of the transmissions communicated between the integrated circuit and the electronic component in response to the communication of each of the transmissions,

means for calibrating the external clock delay as a function of the recorded timing parameters for each of the transmissions to support future communications between the integrated circuit and the electronic component; and

means for generating a feedback clock on the integrated circuit, the feedback clock having a programmable delay from the system clock, and wherein the communications between the integrated circuit and the electronic component further comprise using the external clock to write to and read from the electronic component, and using the feedback clock to sample, at the integrated circuit, data read from the electronic component, wherein

the external clock delay and the feedback clock delay are programmed with a fixed offset there between for each of read/write operations, and wherein the external clock delay and the feedback clock delay are calibrated with the fixed offset there between, wherein the calibration of the external clock delay and the feedback clock delay further comprises determining the lowest delay between the system clock and one of the external and feedback clocks for the successful read/write operation and the highest delay between the system clock and said one of the external and feedback clock for a successful read/write operation, and selecting a delay comprising the center value between the lowest delay and the highest delay, the selected delay being used to calibrate said one of the external and feedback clocks.